

# FC41D Hardware Design

#### Wi-Fi&Bluetooth Module Series

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# **Safety Information**

The following safety precautions must be observed during all phases of operation, such as usage, service or repair of any cellular terminal or mobile incorporating the module. Manufacturers of the cellular terminal should notify users and operating personnel of the following safety information by incorporating these guidelines into all manuals of the product. Otherwise, Quectel assumes no liability for customers' failure to comply with these precautions.



Full attention must be paid to driving at all times in order to reduce the risk of an accident. Using a mobile while driving (even with a handsfree kit) causes distraction and can lead to an accident. Please comply with laws and regulations restricting the use of wireless devices while driving.



Switch off the cellular terminal or mobile before boarding an aircraft. The operation of wireless appliances in an aircraft is forbidden to prevent interference with communication systems. If there is an Airplane Mode, it should be enabled prior to boarding an aircraft. Please consult the airline staff for more restrictions on the use of wireless devices on an aircraft.



Wireless devices may cause interference on sensitive medical equipment, so please be aware of the restrictions on the use of wireless devices when in hospitals, clinics or other healthcare facilities.



Cellular terminals or mobiles operating over radio signal and cellular network cannot be guaranteed to connect in certain conditions, such as when the mobile bill is unpaid or the (U)SIM card is invalid. When emergent help is needed in such conditions, use emergency call if the device supports it. In order to make or receive a call, the cellular terminal or mobile must be switched on in a service area with adequate cellular signal strength. In an emergency, the device with emergency call function cannot be used as the only contact method considering network connection cannot be guaranteed under all circumstances.



The cellular terminal or mobile contains a transceiver. When it is ON, it receives and transmits radio frequency signals. RF interference can occur if it is used close to TV sets, radios, computers or other electric equipment.



In locations with explosive or potentially explosive atmospheres, obey all posted signs and turn off wireless devices such as mobile phone or other cellular terminals. Areas with explosive or potentially explosive atmospheres include fuelling areas, below decks on boats, fuel or chemical transfer or storage facilities, and areas where the air contains chemicals or particles such as grain, dust or metal powders.



# **About the Document**

# **Revision History**

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-	2022-07-18	Soni RAO/Michael DU	Creation of the document	
1.0	2022-08-23	Soni RAO/Michael DU	First official release	



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# 1 Introduction

This document defines the FC41D and describes its air interface and hardware interfaces which are connected with your application.

With this document, you can quickly understand module interface specifications, electrical and mechanical details, as well as other related information of the module. The document, coupled with application notes and user guides, makes it easy to design and set up mobile applications with the module.

#### 1.1. Special Mark

**Table 1: Special Mark** 

Mark	Definition
	When an asterisk (*) is used after a function, feature, interface, pin name, AT command, or
*	argument, it indicates that the function, feature, interface, pin name, AT command, or argument is under development and currently not supported, unless otherwise specified.



# **2** Product Concept

#### 2.1. General Description

FC41D is a low-power, cost-effective Bluetooth 5.2 and IEEE 802.11b/g/n module, which integrates the hardware and software resources required for Wi-Fi and Bluetooth applications. It can support AP and STA of Wi-Fi connection, and low-power Bluetooth connection. It is very suitable for low-speed applications and data acquisition applications such as home intelligent terminal, industrial application and so on.

FC41D has a built-in Wi-Fi and Bluetooth ultra-high integration microcontroller, which provides the necessary ability to calculate and stable Wi-Fi and Bluetooth connectivity for IoT data terminals. It includes:

- 120 MHz ARM kernel
- 256 KB RAM
- 2 MB Flash
- Complies with IEEE 802.11b/g/n and Bluetooth 5.2 standards

### 2.2. Key Features

The following table describes the key features of FC41D.

**Table 2: Key Features** 

Features	Details		
	VBAT Power Supply:		
Power Supply	<ul> <li>Supply voltage range: 3.0–3.6 V</li> </ul>		
	<ul> <li>Typical supply voltage: 3.3 V</li> </ul>		
Operating Frequency	• Wi-Fi: 2.412–2.484 GHz		
Operating Frequency	<ul> <li>Bluetooth: 2.402–2.480 GHz</li> </ul>		
Wi-Fi Transmission Data	802.11b: 1 Mbps, 2 Mbps, 5.5 Mbps, 11 Mbps		
Rates	• 802.11g: 6 Mbps, 9 Mbps, 12 Mbps, 18 Mbps, 24 Mbps, 36 Mbps,		



	48 Mbps, 54 Mbps
	• 802.11n: HT20 (MCS0–MCS7)
Wi-Fi Transmitting Power	<ul> <li>2.4 GHz:</li> <li>802.11b/11 Mbps: 16 dBm</li> <li>802.11g/54 Mbps: 14 dBm</li> <li>802.11n/HT20 MCS7: 13 dBm</li> </ul>
Wi-Fi Protocol Features	IEEE 802.11b/g/n
Wi-Fi Modulation	CCK, BPSK, QPSK,16QAM, 64QAM
Wi-Fi Operation Mode	<ul><li>AP</li><li>STA</li></ul>
Bluetooth Protocol Feature	GATT
Bluetooth Operation Mode	BLE
Bluetooth Modulation	GFSK
Wireless Application Interfaces	<ul> <li>Main UART: Used for AT command communication, data transmission and firmware upgrade</li> <li>Debug UART: Used for the output of partial logs</li> <li>SPI*: Supports one SPI interface and master and slave modes</li> </ul>
Antenna Interface	<ul> <li>PCB antenna</li> <li>IPEX antenna (Optional)</li> <li>Wi-Fi/Bluetooth antenna interface (ANT_WIFI/BT), 50 Ω impedance (Optional)</li> </ul>
Physical Characteristics	<ul> <li>Package: LCC</li> <li>Weight: 1.51 g</li> <li>Size: (20.0 ±0.2) mm × (18.0 ±0.2) mm × (2.6 ±0.2) mm</li> </ul>
Temperature Range	<ul> <li>Operating temperature range ¹: -40 °C to +85 °C</li> <li>Storage temperature range: -45 °C to +95 °C</li> </ul>
RoHS	All hardware components are fully compliant with EU RoHS directive

<sup>&</sup>lt;sup>1</sup> Within the operating temperature range, the module's related performance meets IEEE and Bluetooth specifications.



# 2.3. Functional Diagram

The following figure shows a block diagram of FC41D.

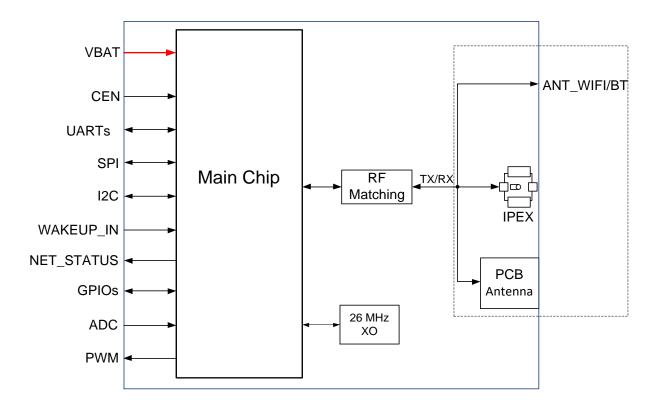


Figure 1: Functional Diagram

NOTE

FC41D supports PCB antenna by default; IPEX antenna and ANT\_WIFI/BT are optional.

#### 2.4. EVB

Quectel supplies an evaluation board (FC41D TE-B) with accessories to control or test the module. For more details, see *document* [1].



# **3** Application Interfaces

# 3.1. General Description

The FC41D has 27 LCC pins. The following interfaces are described in detail in subsequent chapters:

- Power supply
- Module reset
- Wireless connectivity interfaces
  - UART interfaces
  - SPI interface\*
- I2C interface\*
- PWM interface\*
- WAKEUP interface
- Network status indication
- GPIO interfaces\*
- ADC interface\*
- RF antenna interface



#### 3.2. Pin Assignment

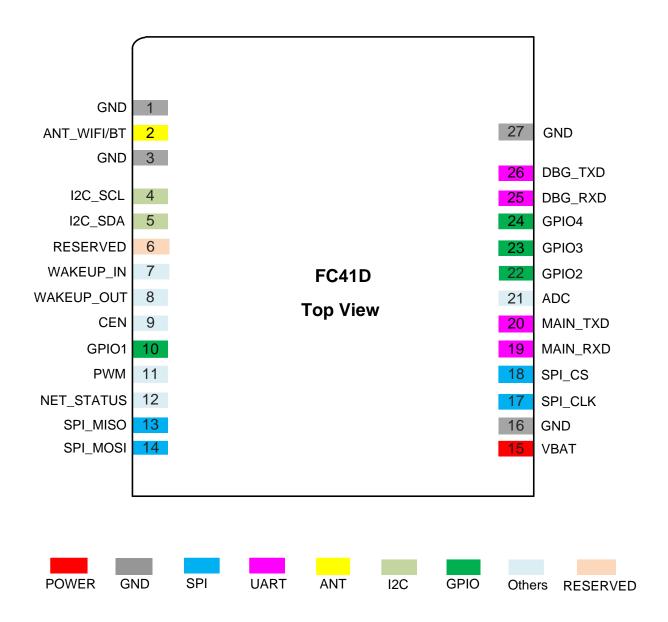


Figure 2: Pin Assignment (Top View)

**NOTE** 

Keep all RESERVED and unused pins open.



# 3.3. Pin Description

The following tables show the pin description of module.

**Table 3: I/O Parameter Description** 

**Table 4: Pin Description** 

Power Supply					
Pin Name	Pin No.	I/O	Description	DC Characteristics	Comment
VBAT	15	PI	Power supply for the module	Vmax = 3.6 V Vmin = 3.0 V Vnom = 3.3 V	It must be provided with sufficient current up to 0.3 A.
GND	1, 3, 16,	27			
Reset					
Pin Name	Pin No.	I/O	Description	DC Characteristics	Comment
CEN	9	DI	Resets the module	Vmax = 3.6 V Vmin = 3.0 V Vnom = 3.3 V	Internally pulled up to 3.3 V. Hardware reset; active low.
Main UART					
Pin Name	Pin No.	I/O	Description	DC Characteristics	Comment



MAIN_TXD         20         DO         Main UART transmits dand UART receives         3.3 V           Debug UART         Debug UART receives         3.3 V           DBG_TXD         26         DO         Debug UART receives         3.3 V           DBG_RXD         25         DI         Debug UART receives         3.3 V           SPI Interface*           Pin Name         Pin No.         I/O         Description         DC Characteristics         Comment           SPI_MISO         13         DIO         SPI master input salve output salve output slave input slave mode, it's an input signal; in slave mode, it's an output signal; in slave mode, it's an output signal.           IZC Interface*           Pin Name         Pin No.         I/O         Description         DC Characteristics         Comment           I2C_SCL         4         OD         I2C serial clock gradedata         3.3 V         Requires external pull-up to 3.3 V.           WAKEUP Interface*         Wakes up the module from deep sleep or standby mode         Wakes up the module from deep sleep or standby mode         Rising edge wakeup.           WAKEUP_OUT         8         <						
MAIN_RXD 19 DI Main UART receives    Pin Vame   Pin No.   I/O   Description   DC Characteristics   Dispansion in plan to signal; in slave mode, it's an input signal. In master mode, it's an input signal; in slave mode, it's an input signal. In master mode, it's an input signal, in slave mode, it's an input signal. In master mode, it's an input signal, in slave mode, it's an input signal. In master mode, it's an input signal, in slave mode, it's an input signal, in slave mode, it's an input signal, in slave mode, it's an input signal. In master mode, it's an input signal, in slave mode, it's an input signal, in slave mode, it's an input signal.   In master mode, it's an output signal, in slave mode, it's an input signal, in slave mode, it's an input signal, in slave mode, it's an output signal.   In master mode, it's an output signal, in slave mode, it's an input signal, in slave mode, it's an input signal, in slave mode, it's an output signal.   In master mode, it's an output signal, in slave mode, it's an input signal, in slave mode, it's an output signal, in slave mode, it's an output signal.   In master mode, it's an output signal, in slave mode, it's an o	MAIN_TXD	20	DO		221/	
DBG_TXD 26 DO Debug UART transmits  DBG_RXD 25 DI Debug UART receives  SPI_Interface*  Pin Name Pin No. I/O Description DC Characteristics Comment  SPI_MISO 13 DIO SPI master input salve output slave input signal; in slave mode, it's an input signal. In master mode, it's an input signal. In master mode, it's an input signal, in slave mode, it's an output signal; in slave mode, it's an output signal.  IZC Interface*  Pin Name Pin No. I/O Description DC Characteristics Comment  IZC_SCL 4 OD I2C serial clata  WAKEUP Interface  Pin Name Pin No. I/O Description DC Characteristics Comment  WAKEUP Interface  WAKEUP_IN 7 DI Wakes up the module from deep sleep or standby mode  WAKEUP_OUT 8 DO Wakes up the host	MAIN_RXD	19	DI		- J.J V	
DBG_IXD 26 DO transmits DBG_RXD 25 DI Debug UART receives  SPI Interface*  Pin Name Pin No. I/O Description DC Characteristics Comment  SPI_MISO 13 DIO SPI master input salve output SPI_MOSI 14 DIO SPI master output slave input  SPI_CLK 17 DIO SPI clock 3.3 V  SPI_CLK 17 DIO SPI chip select In master mode, it's an output signal; in slave mode, it's an input signal. In master mode, it's an input signal. In master mode, it's an output signal. In master mode, it's an output signal.  ID MASTER MAST	Debug UART					
DBG_RXD 25 DI Debug UART receives  SPI Interface*  Pin Name Pin No. I/O Description DC Characteristics Comment  SPI_MISO 13 DIO SPI master input salve output  SPI_MOSI 14 DIO SPI clock IT an output silave input  SPI_CLK IT DIO SPI clock IT an input signal; in slave mode, it's an output signal.  In master mode, it's an input signal; in slave mode, it's an input signal.  IL master mode, it's an output signal.  In mas	DBG_TXD	26	DO	_	0.01/	
Pin Name       Pin No.       I/O       Description       DC Characteristics       Comment         SPI_MISO       13       DIO       SPI master input salve output salve output salve output slave input       A SPI master output salve input       In master mode, it's an output signal; in slave mode, it's an input signal.         SPI_CLK       17       DIO       SPI clock       3.3 V       In master mode, it's an output signal. In master mode, it's an input signal.         SPI_CS       18       DIO       SPI chip select       In master mode, it's an input signal.         IZC Interface*         Pin Name       Pin No.       I/O       Description       DC Characteristics       Comment         I2C_SCL       4       OD       I2C serial clock       3.3 V       Requires external pull-up to 3.3 V.         WAKEUP Interface*       Pin No.       I/O       Description       DC Characteristics       Comment         WAKEUP_IN       7       DI       Wakes up the module from deep sleep or standby modele from deep sleep or standby mode	DBG_RXD	25	DI	· ·	- 3.3 V	
SPI_MISO 13 DIO SPI master input salve output  SPI_MOSI 14 DIO SPI master output slave input  SPI_CLK 17 DIO SPI clock 3.3 V  SPI_CCLK 17 DIO SPI clock 3.3 V  In master mode, it's an input signal; in slave mode, it's an input signal. In master mode, it's an input signal. In master mode, it's an input signal. In master mode, it's an output signal.  In master mode, it's an input signal. In master mode, it's an input signal.  In master mode, it's an input signal. In master mode, it's an output signal.  ICC Interface*  Pin Name Pin No. I/O Description DC Characteristics Comment  I2C_SCL 4 OD I2C serial clock 3.3 V  WAKEUP Interface*  Pin Name Pin No. I/O Description DC Characteristics Comment  WAKEUP_IN 7 DI Wakes up the module from deep sleep or standby mode  Wakes up the module from deep sleep or standby mode  WAKEUP_OUT 8 DO Wakes up the host Active high.	SPI Interface*					
SPI_MISO 13 DIO salve output SPI_MOSI 14 DIO SPI master output slave input  SPI_CLK 17 DIO SPI clock 3.3 V  In master mode, it's an output signal; in slave mode, it's an input signal. In master mode, it's an input signal. In master mode, it's an input signal. In master mode, it's an output signal. In master mode, it's an output signal.  IZC Interface*  Pin Name Pin No. I/O Description DC Characteristics Comment  I2C_SCL 4 OD I2C serial clock 12C_SDA 5 OD I2C serial data  WAKEUP Interface*  Pin Name Pin No. I/O Description DC Characteristics Comment  WAKEUP Interface*  Wakes up the module from deep sleep or standby mode  WAKEUP_OUT 8 DO Wakes up the host  Wakes up the host  Wakes up the host	Pin Name	Pin No.	I/O	Description	DC Characteristics	Comment
SPI_MOSI 14 DIO slave input  SPI_CLK 17 DIO SPI clock  SPI_CCLK 17 DIO SPI clock  SPI_CCS 18 DIO SPI chip select  SPI_CCS IN Master mode, it's an input signal.  SPI_CCS IN MASTER MA	SPI_MISO	13	DIO	•	_	
SPI_CLK 17 DIO SPI clock 3.3 V an output signal; in slave mode, it's an input signal. In master mode, it's an input signal. In master mode, it's an input signal. In master mode, it's an input signal.  ICC Interface*  Pin Name Pin No. I/O Description DC Characteristics Comment  I2C_SCL 4 OD I2C serial clock 12C_SDA 5 OD I2C serial data  WAKEUP Interface*  Pin Name Pin No. I/O Description DC Characteristics Comment  Wakeup Interface*  Active high.	SPI_MOSI	14	DIO	•	_	
SPI_CS 18 DIO SPI chip select slave mode, it's an output signal; in slave mode, it's an output signal.  I2C Interface*  Pin Name Pin No. I/O Description DC Characteristics Comment  I2C_SCL 4 OD I2C serial clock I2C_SDA 5 OD I2C serial data  WAKEUP Interface*  Pin Name Pin No. I/O Description DC Characteristics Comment  Wakes up the module from deep sleep or standby mode  WAKEUP_OUT 8 DO Wakes up the host  Wakes up the host  Wakes up the host  Wakes up the host  Active high.	SPI_CLK	17	DIO	SPI clock	3.3 V	an output signal; in slave mode, it's an
Pin Name       Pin No.       I/O       Description       DC Characteristics       Comment         I2C_SCL       4       OD       I2C serial clock       3.3 V       Requires external pull-up to 3.3 V.         I2C_SDA       5       OD       I2C serial data       JUL violation       DC Characteristics       Comment         WAKEUP Interface       Wakes up the module from deep sleep or standby mode       Name       Rising edge wakeup.         WAKEUP_IN       7       DI       Wakes up the module from deep sleep or standby mode       3.3 V         WAKEUP_OUT       8       DO       Wakes up the host       Active high.	SPI_CS	18	DIO	SPI chip select	-	an input signal; in slave mode, it's an
I2C_SCL 4 OD I2C serial clock I2C_SDA 5 OD I2C serial data  WAKEUP Interface  Pin Name Pin No. I/O Description DC Characteristics Comment  WAKEUP_IN 7 DI Wakes up the module from deep sleep or standby mode  WAKEUP_OUT 8 DO Wakes up the host Active high.	I2C Interface*					
I2C_SDA   5   OD   I2C serial data   3.3 V   Requires external pull-up to 3.3 V.	Pin Name	Pin No.	I/O	Description	DC Characteristics	Comment
WAKEUP Interface  Pin Name Pin No. I/O Description Wakes up the module from deep sleep or standby mode  WAKEUP_OUT  8 DO Wakes up the host  Wakes up the host  Wakes up the host  Rising edge wakeup.  Active high.	I2C_SCL	4	OD	I2C serial clock	0.01/	Requires external
Pin Name       Pin No.       I/O       Description       DC Characteristics       Comment         WAKEUP_IN       7       DI       Wakes up the module from deep sleep or standby mode       Rising edge wakeup.         WAKEUP_OUT       8       DO       Wakes up the host       Active high.	I2C_SDA	5	OD	I2C serial data	- 3.3 V	pull-up to 3.3 V.
WAKEUP_IN 7 DI Wakes up the module from deep sleep or standby mode 3.3 V  WAKEUP_OUT 8 DO Wakes up the host Active high.	WAKEUP Interfa	се				
WAKEUP_IN 7 DI module from deep sleep or standby mode 3.3 V  WAKEUP_OUT 8 DO Wakes up the host Active high.	Pin Name	Pin No.	I/O	Description	DC Characteristics	Comment
·	WAKEUP_IN	7	DI	module from deep sleep or standby	3.3 V	
Indication Interface	WAKEUP_OUT	8	DO	Wakes up the host		Active high.
	Indication Interfa	ace				



Pin Name	Pin No.	I/O	Description	DC Characteristics	Comment
NET_STATUS	12	DO	Indicates the module's network activity status	3.3 V	Outputs high level when Wi-Fi is connected in STA mode.
PWM Interface*					
Pin Name	Pin No.	I/O	Description	DC Characteristics	Comment
PWM	11	DO	Pulse width modulation output channel	3.3 V	
GPIO Interface*					
Pin Name	Pin No.	I/O	Description	DC Characteristics	Comment
GPIO1	10	DIO	General-purpose input/output	_	
GPIO2	22	DIO	General-purpose input/output	- - 3.3 V	Wake-up interrupt
GPIO3	23	DIO	General-purpose input/output		тике-ир ппетирг.
GPIO4	24	DIO	General-purpose input/output		
ADC Interface*					
Pin Name	Pin No.	I/O	Description	DC Characteristics	Comment
ADC	21	Al	General-purpose ADC interface	Voltage range: 0–2.4 V	
RF Antenna Inte	rface				
Pin Name	Pin No.	I/O	Description	DC Characteristics	Comment
ANT_WIFI/BT	2	AIO	Wi-Fi/Bluetooth antenna interface		50 Ω impedance.
RESERVED					
Pin Name	Pin No.	I/O	Description	DC Characteristics	Comment
RESERVED	6		RESERVED		Keep it open.



#### 3.4. Power Supply Design

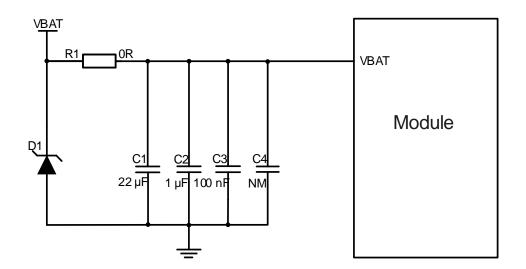
The following table shows the definition of power supply pin and ground pins of FC41D.

Table 5: Pin Definition of Power Supply and GND Pins

Pin Name	Pin No.	Description	Min.	Тур.	Max.	Unit
VBAT	15	Power supply	3.0	3.3	3.6	V
GND	1, 3, 16, 27	Ground				

FC41D is powered by VBAT, and it is recommended to use a power supply chip that can provide at least 0.3 A output current. To ensure better power supply performance, it is recommended to parallel 22  $\mu$ F decoupling capacitor, and 1  $\mu$ F and 100 nF filter capacitor near the module's VBAT pin. Meanwhile, it is recommended to add a TVS near the VBAT to improve the surge voltage bearing capacity of the module. In principle, the longer the VBAT line is, the wider it should be.

VBAT reference circuit is shown as below:



**Figure 3: VBAT Reference Circuit** 

After the module VBAT is powered on, keep the CEN pin at high level to realize the automatic startup of the module.



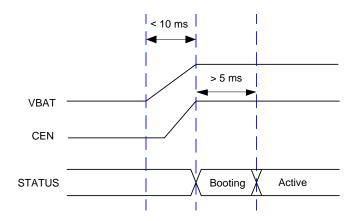


Figure 4: Power-up Timing

Cut off the power supply of VBAT, the module will automatically execute power-off procedure.

#### 3.5. Reset

Drive CEN low for at least 100 ms and then release it to reset the module.

**Table 6: Pin Definition of Reset Pin** 

Pin Name	Pin No.	Description	Comment
CEN	9	Reset the module	Pulled up to 3.3 V internally.

The reference designs for resetting the module are shown below. An open drain/collector driving circuit or a button can be used to control the CEN pin.

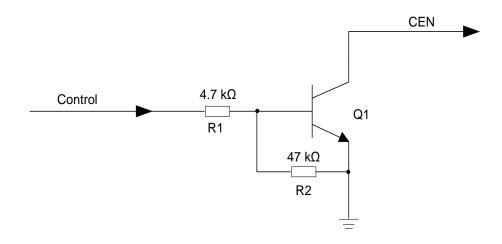


Figure 5: Reference Circuit of CEN by Using Driving Circuit



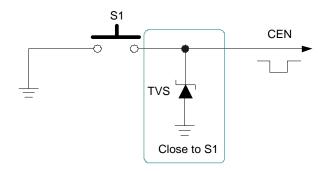


Figure 6: Reference Circuit of CEN by Using Button

The reset scenario is illustrated in the following figure.

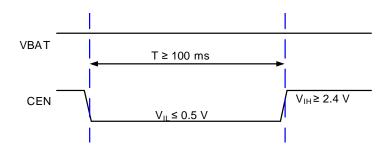


Figure 7: Timing of Resetting the Module

#### 3.6. Wireless Connectivity Interfaces

#### 3.6.1. UART Interfaces

The module provides two UART interfaces: the main UART and the debug UART. The module is used as DCE (Data Communication Equipment), and is connected in the traditional DCE-DTE (Data Terminal Equipment) mode.

**Table 7: Pin Definition of UART Interfaces** 

Pin Name	Pin No.	I/O	Description
MAIN_TXD	20	DO	Main UART transmits data
MAIN_RXD	19	DI	Main UART receives data
DBG_TXD	26	DO	Debug UART transmits data
DBG_RXD	25	DI	Debug UART receives data



The main UART can be used for AT command communication and data transmission. The default baud rate is 115200 bps, and the maximum baud rate can reach 2 Mbps.

The main UART is also available for firmware upgrade and supports a default baud rate of 921600 bps.

The following is the schematic diagram of the main UART interface connection between DCE and DTE.

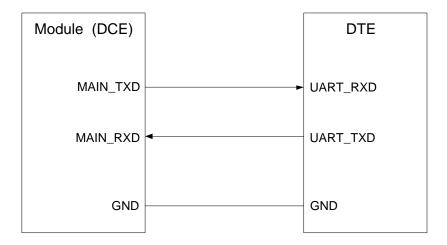


Figure 8: Main UART Connection Diagram

The debug UART interface supports 115200 bps baud rate by default, and is used for the output of partial logs.

The following is a reference design of debug UART.

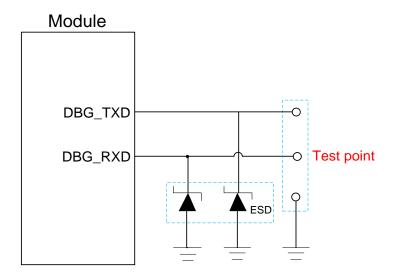


Figure 9: Debug UART Reference Circuit



#### 3.6.2. SPI Interface\*

FC41D provides a SPI interface that supports both master and slave modes. The maximum clock frequency of the interface can reach 50 MHz in slave mode, and 8 MHz in the master mode.

The pin description of SPI interface is shown as below:

**Table 8: Pin Definition of SPI Interface** 

Pin Name	Pin No.	I/O	Description	Comment
SPI_MISO	13	DIO	SPI master input slave output	
SPI_MOSI	14	DIO	SPI master output slave input	
SPI_CLK	17	DIO	SPI clock	In master mode, it's an output signal; in slave mode, it's an input signal.
SPI_CS	18	DIO	SPI chip select	In master mode, it's an input signal; in slave mode, it's an output signal.

#### 3.7. I2C Interface\*

FC41D provides an I2C interface that supports master mode only with maximum clock frequency of 400 kHz and 7-bit addressing. It can be used to connect peripherals such as EEPROM.

Table 9: Pin Definition of I2C Interface

Pin Name	Pin No.	I/O	Description	Comment	
I2C_SCL	4	OD	I2C serial clock	Require external	
I2C_SDA	5	OD	I2C serial data	pull-up to 3.3 V.	



#### 3.8. PWM Interface\*

FC41D provides 1 PWM channel by default. The following table shows the pin description of PWM interface.

**Table 10: Pin Definition of PWM Interface** 

Pin Name	Pin No.	I/O	Description
PWM	11	DO	Pulse width modulation output channel

#### 3.9. WAKEUP Interface

WAKEUP\_IN pin can wake up the module from deep sleep mode or standby mode, while WAKEUP\_OUT pin can be used to wake up the host.

**Table 11: Pin Definition of WAKEUP Interface** 

Pin Name	Pin No.	1/0	Description	Comment
WAKEUP_IN	7	DI	Wake up the module from deep sleep or standby mode	Rising edge wakeup.
WAKEUP_OUT	8	DO	Wake up the host	Active high.

#### 3.10. Network Status Indication

The network indication pin NET\_STATUS can drive the network status indicators.

The following table describes the pin definition and logic level changes of NET\_STATUS.

**Table 12: Pin Definition of NET\_STATUS** 

Pin Name	Pin No.	I/O	Description	Comment
NET_STATUS	12	DO	Indicate the module's network activity status.	Outputs high level when Wi-Fi is connected in STA mode.



A reference circuit is shown in the following figure.

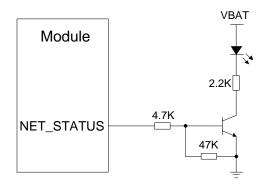


Figure 10: Reference Circuit of the Network Status Indicator

#### 3.11. GPIO Interfaces\*

FC41D provides 4 GPIO interfaces by default. The following table shows the pin description of GPIO.

**Table 13: Pin Definition of GPIO Interfaces** 

Pin Name	Pin No.	1/0	Description	Comment
GPIO1	10			
GPIO2	22	- DIO	General-purpose	Maka un internut
GPIO3	23		input/output	Wake-up interrupt.
GPIO4	24			



#### 3.12. ADC Interface\*

The module provides one ADC interface by default, and the voltage range is 0–2.4 V. To improve the accuracy of ADC, surround the trace of ADC with ground.

**Table 14: Pin Definition of ADC Interface** 

Pin Name	Pin No.	I/O	Description
ADC	21	Al	General-purpose ADC interface

**Table 15: ADC Features** 

Parameter	Min.	Тур.	Max.	Unit
ADC Voltage Range	0	-	2.4	V
ADC Resolution Rate	-	TBD	-	bit
ADC Sample Rate	-	TBD	-	MHz

#### 3.13. RF Antenna Interface

FC41D provides PCB antenna, IPEX connector and ANT\_WIFI/BT (stamp hole). The IPEX connector is not mounted on the module when using PCB antenna or ANT\_WIFI/BT. FC41D supports PCB antenna by default; IPEX antenna and ANT\_WIFI/BT are optional.

#### 3.13.1. Operating Frequency

The operating frequency of FC41D is shown in the table below:

**Table 16: FC41D Operating Frequency** 

Mode	Frequency	Unit
2.4 GHz Wi-Fi	2.412–2.484	GHz
Bluetooth	2.402–2.480	GHz



#### 3.13.2. RF Antenna Pin Description (Optional)

RF Antenna pin description is as below:

**Table 17: Antenna Pin Definition** 

Pin Name	Pin No.	I/O	Description	Comment
ANT_WIFI/BT	2	AIO	Wi-Fi/Bluetooth antenna interface	50 Ω impedance.

The circuit of RF antenna interface is shown below. In order to achieve better RF performance, it is necessary to reserve LC and  $\pi$  matching circuit. Matching components such as R1, L1, C1, C2, C3 and D1 should be placed as close to the antenna as possible, L1, C1, C2, C3 and D1 are not mounted by default. The parasitic capacitance of TVS should be less than 0.05 pF.

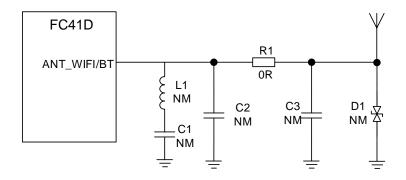


Figure 11: RF Antenna Reference Design

#### 3.13.2.1. Reference Design of RF Layout (Optional)

The characteristic impedance of all RF traces on your PCB should be controlled at  $50~\Omega$ . The impedance of the RF traces is usually determined by the trace width (W), the material's dielectric constant, the height from the reference ground to the signal layer (H), and the spacing between RF traces and grounds (S). The microstrip or coplanar waveguide is typically used in RF layout to control characteristic impedance. The following are reference designs for microstrip or coplanar waveguide transmission lines with different PCB structures.



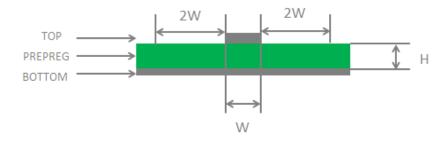


Figure 12: Microstrip Design on a 2-layer PCB

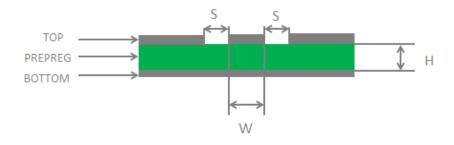


Figure 13: Coplanar Waveguide Design on a 2-layer PCB

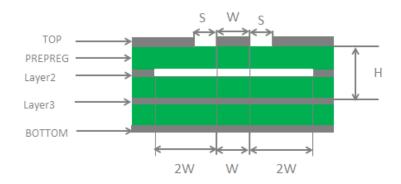


Figure 14: Coplanar Waveguide Design on a 4-layer PCB (Layer 3 as Reference Ground)



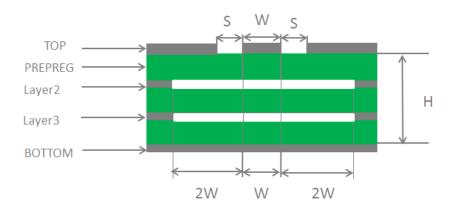


Figure 15: Coplanar Waveguide Design on a 4-layer PCB (Layer 4 as Reference Ground)

To ensure RF performance and reliability, the following principles should be complied with in RF layout design:

- Use an impedance simulation tool to accurately control the characteristic impedance of RF traces to 50 Ω.
- The GND pins adjacent to RF pins should not be designed as thermal relief pads, and should be fully connected to ground.
- The distance between the RF pins and the RF connector should be as short as possible and all the right-angle traces should be changed to curved ones. The recommended trace angle is 135°.
- There should be clearance under the signal pin of the antenna connector or solder joint.
- The reference ground of RF traces should be complete. Meanwhile, adding some ground vias around RF traces and the reference ground could help to improve RF performance. The distance between the ground vias and RF traces should be no less than two times the width of RF signal traces (2 x W).
- Keep RF traces away from interference sources, and avoid intersection and paralleling between traces on adjacent layers.

For more details about RF layout, see document [2].

#### 3.13.3. On Board PCB Antenna

**Table 18: On Board PCB Antenna Characteristics** 

Characters	Min.	Тур.	Max.	Unit
Frequency	2400	-	2500	MHz
Impedance	-	50	-	Ω
VSWR	-	-	3	-



Gain	-	-1.81	-	dBi
Efficiency	-	35 %	-	-

When using the PCB antenna on the module, the module should be placed at the side of the motherboard, and the distance of keepout between PCB antenna to GND of motherboard should be at least 3 mm, and the distance between PCB antenna to connectors, pin headers, ethernet port and any other metal components on the motherboard should be at least 16 mm. All layers in the PCB of the motherboard under the PCB antenna should be designed as keepout area.

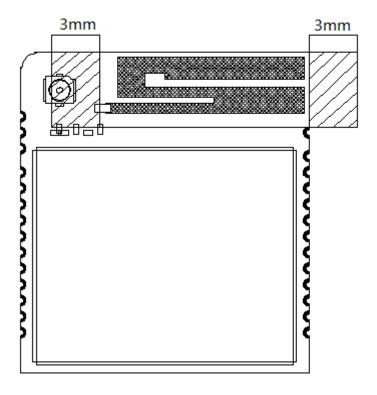


Figure 16: Keepout Area on Motherboard



#### 3.13.4. IPEX Connector (Optional)

The mechanic size of the IPEX connector (MPN: 20579-001E, MHF® 4L Receptacle) provided by the FC41D is as follows.

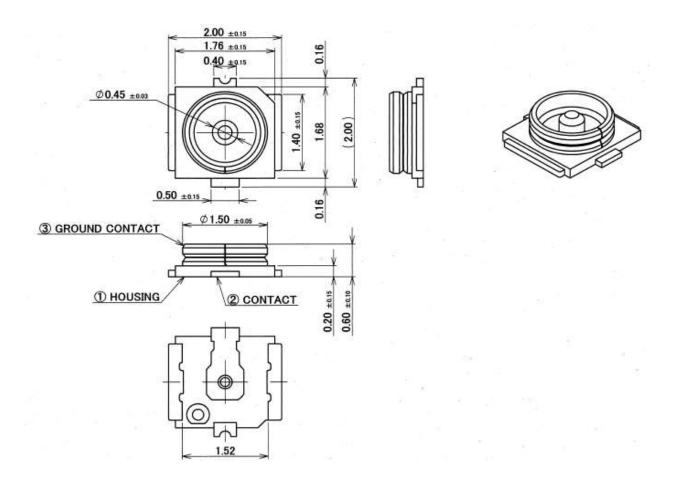


Figure 17: IPEX Connector Size



#### 3.13.5. Antenna Cable and Antenna Requirements

**Table 19: Antenna Cable Requirement** 

Frequency	Requirement
2.412–2.484 GHz	Insertion loss <1 dB

#### **Table 20: Antenna Requirement**

Туре	Requirement
Frequency	2.412–2.484 GHz
VSWR	< 2
Gain (dBi)	Тур. 1
Max. input power (W)	50
Input impedance (Ω)	50
Polarization type	Vertical



# 4 Reliability, Radio and Electrical Characteristics

### 4.1. Absolute Maximum Ratings

Absolute maximum ratings for power supply and voltage on digital and analog pins of the module are listed in the following table.

**Table 21: Absolute Maximum Ratings** 

Parameter	Min.	Max.	Unit
VBAT	-0.3	3.9	V
I/O input voltage	-0.3	3.9	V

# 4.2. Power Supply Ratings

**Table 22: Module Power Supply Ratings** 

Parameter	Min.	Тур.	Max.	Unit
VBAT	3.0	3.3	3.6	V



# 4.3. Digital I/O Characteristics

Table 23: Digital I/O Requirements

Parameter	Description	Min.	Max.	Unit
V <sub>IH</sub>	High Level Input Voltage	0.7 × VBAT	VBAT + 0.2	V
V <sub>IL</sub>	Low Level Input Voltage	-0.3	0.3 × VBAT	V
V <sub>OH</sub>	High Level Output Voltage	0.9 × VBAT	VBAT	V
V <sub>OL</sub>	Low Level Output Voltage	0	0.1 × VBAT	V
l <sub>iL</sub>	Input Leakage Current	-5	5	μΑ

# 4.4. Power Consumption

#### 4.4.1. Power Consumption in Low Power Modes

**Table 24: Power Consumption in Low Power Modes** 

Parameter	Description	Тур.	Unit
Deep sleep mode	AT+QDEEPSLEEP can set the module to deep sleep mode. In this case, the serial interfaces stop working and software settings are not saved.	8.6	μΑ
Standby mode	AT+QLOWPOWER can set the module to standby mode. In this case, the serial interfaces stop working but software settings can be saved.	30	μΑ
Idle state	Neither Wi-Fi nor Bluetooth does any operation.	22.74	mA



For more information about AT command, please refer to document [4].



#### 4.4.2. Power Consumption in Normal Operating Modes

**Table 25: Power Consumption in Normal Operating Modes** 

Parameter	Description	Тур.	Unit
Wi-Fi Scan	Scan in every 2 s	68.59	mA
	STA mode is ON, but no STA device is connected	74.52	mA
1411 = 1 0	SoftAP mode is ON, and 1 STA device is connected	77.11	mA
Wi-Fi Connected	SoftAP mode is ON, and 2 STA devices is connected	77.29	mA
	SoftAP mode is ON, but no STA device is connected	77.09	mA
	SoftAP mode data transmission	155.29	mA
	STA mode data transmission	147.81	mA
Data Transmission	SoftAP mode + BLE Server mode data transmission	157.56	mA
	STA mode + BLE Server mode data transmission	149.66	mA
	Receive data as Server	28.41	mA
Divistantly Compared	Transmit data as Server	28.39	mA
Bluetooth Connected	Receive data as Client	23.68	mA
	Transmit data as Client	23.68	mA
	802.11b Tx (2.4 GHz) 1 Mbps	91	mA
	802.11b Tx (2.4 GHz) 11 Mbps	92	mA
RF Non-signaling Mode	802.11g Tx (2.4 GHz) 6 Mbps	90	mA
	802.11g Tx (2.4 GHz) 54 Mbps	88	mA
	802.11n Tx (2.4 GHz) HT20 MCS0	89	mA
	802.11n Tx (2.4 GHz) HT20 MCS7	88	mA



#### 4.5. RF Performances

#### 4.5.1. Wi-Fi Performances

Table 26: 2.4 GHz Wi-Fi Conducted Output Power

Operating Mode	Rate	Min. (dBm)	Typ. (dBm)
802.11b	1 Mbps	14	16
802.11b	11 Mbps	14	16
802.11g	6 Mbps	13	15
802.11g	54 Mbps	12	14
802.11n, HT20	MCS0	12	14
802.11n, HT20	MCS7	11	13

Table 27: 2.4 GHz Wi-Fi Conducted Receive Sensitivity

Operating Mode	Rate	Typ. (dBm)
802.11b	1 Mbps	-96
802.11b	11 Mbps	-87
802.11g	6 Mbps	-89
802.11g	54 Mbps	-72
802.11n, HT20	MCS0	-89
802.11n, HT20	MCS7	-70

Table 28: 2.4 GHz Wi-Fi OTA TRP Test

Operating Mode	Rate	Typ. (dBm)
802.11b	1 Mbps	15
802.11b	11 Mbps	15



802.11g	6 Mbps	14	
802.11g	54 Mbps	13	
802.11n, HT20	MCS0	13	
802.11n, HT20	MCS7	12	

Table 29: 2.4 GHz Wi-Fi OTA TIS Test

Operating Mode	Rate	Typ. (dBm)
802.11b	1 Mbps	-94
802.11b	11 Mbps	-85
802.11g	6 Mbps	-88
802.11g	54 Mbps	-71
802.11n, HT20	MCS0	-86
802.11n, HT20	MCS7	-66

#### 4.5.2. BLE Performances

Table 30: BLE Conducted Mode Output Power / Receive Sensitivity

Operating Mode	Output Power (Typ.)	Receive Sensitivity (Typ.)	Unit
BLE (1 MHz)	6	-95	dBm

#### 4.6. ESD Protection

Static electricity occurs naturally and it may damage the module. Therefore, applying proper ESD countermeasures and handling methods is imperative. For example, wear anti-static gloves during the development, production, assembly and testing of the module; add ESD protection components to the ESD sensitive interfaces and points in the product design.



Table 31: ESD Characteristics (Temperature: 25 ℃, Humidity: 45 %)

Tested Interfaces	Contact Discharge	Air Discharge	Unit
VBAT, GND	±4	±8	kV
ANT_WIFI/BT	±4	±8	kV
Other Interfaces	±0.5	±1	kV

#### 4.7. Operating and Storage Temperatures

Table 32: Operating and Storage Temperatures (Unit: °C)

Parameter	Min.	Тур.	Max.
Operating Temperature Range <sup>2</sup>	-40	+25	+85
Storage Temperature Range	-45	-	+95

\_

<sup>&</sup>lt;sup>2</sup> Within the operating temperature range, the module's related performance meets IEEE and Bluetooth specifications.



### **5** Mechanical Information

This chapter describes the mechanical dimensions of the module. All dimensions are measured in millimeter (mm), and the dimensional tolerances are ±0.2 mm unless otherwise specified.

#### 5.1. Mechanical Dimensions

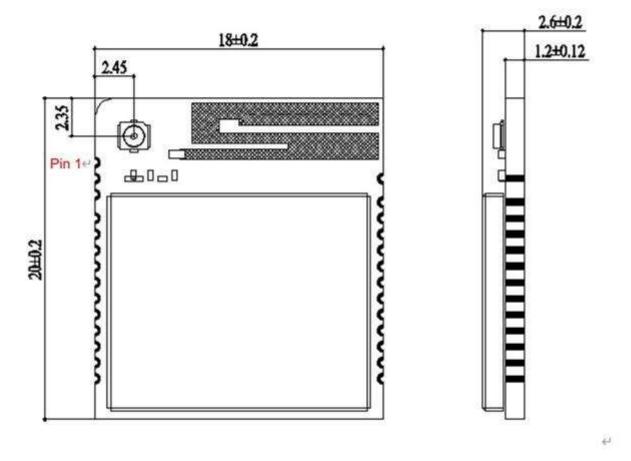


Figure 18: Module Top and Side Dimensions



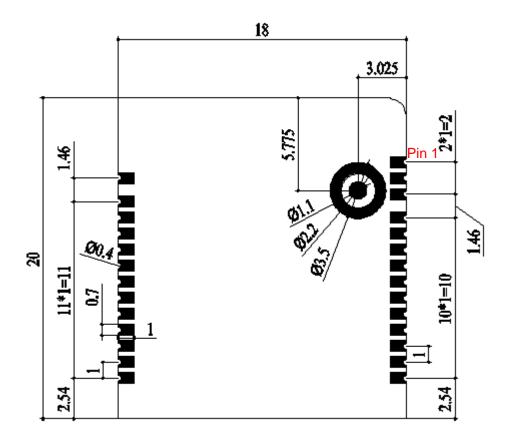


Figure 19: Module Dimension (Bottom View)

NOTE

The package warpage level of the module conforms to the *JEITA ED-7306* standard.



#### 5.2. Recommended Footprint

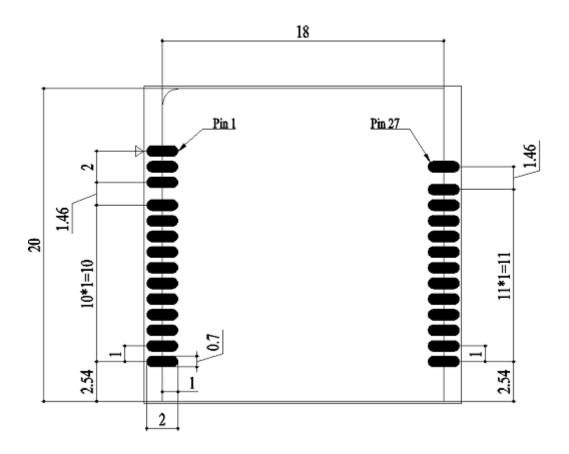


Figure 20: Recommended Footprint (Top View)

**NOTE** 

Keep at least 3 mm between the module and other components on the motherboard to improve soldering quality and maintenance convenience.



#### 5.3. Top and Bottom Views



Figure 21: Top and Bottom Views of the Module

#### **NOTE**

Images above are for illustration purpose only and may differ from the actual module. For authentic appearance and label, please refer to the module received from Quectel.



# **6** Storage, Manufacturing and Packaging

#### **6.1. Storage Conditions**

The module is provided with vacuum-sealed packaging. MSL of the module is rated as 3. The storage requirements are shown below.

- 1. Recommended Storage Condition: the temperature should be 23 ±5 °C and the relative humidity should be 35–60 %.
- 2. Shelf life (in a vacuum-sealed packaging): 12 months in Recommended Storage Condition.
- 3. Floor life: 168 hours <sup>3</sup> in a factory where the temperature is 23 ±5 °C and relative humidity is below 60 %. After the vacuum-sealed packaging is removed, the module must be processed in reflow soldering or other high-temperature operations within 168 hours. Otherwise, the module should be stored in an environment where the relative humidity is less than 10 % (e.g., a dry cabinet).
- 4. The module should be pre-baked to avoid blistering, cracks and inner-layer separation in PCB under the following circumstances:
  - The module is not stored in Recommended Storage Condition;
  - Violation of the third requirement mentioned above;
  - Vacuum-sealed packaging is broken, or the packaging has been removed for over 24 hours;
  - Before module repairing.
- 5. If needed, the pre-baking should follow the requirements below:
  - The module should be baked for 8 hours at 120 ±5 °C;
  - The module must be soldered to PCB within 24 hours after the baking, otherwise it should be put in a dry environment such as in a dry cabinet.

<sup>&</sup>lt;sup>3</sup> This floor life is only applicable when the environment conforms to *IPC/JEDEC J-STD-033*. It is recommended to start the solder reflow process within 24 hours after the package is removed if the temperature and moisture do not conform to, or are not sure to conform to *IPC/JEDEC J-STD-033*. And do not remove the packages of tremendous modules if they are not ready for soldering.



#### NOTE

- 1. To avoid blistering, layer separation and other soldering issues, extended exposure of the module to the air is forbidden.
- 2. Take out the module from the package and put it on high-temperature-resistant fixtures before baking. If shorter baking time is desired, see *IPC/JEDEC J-STD-033* for the baking procedure.
- 3. Pay attention to ESD protection, such as wearing anti-static gloves, when touching the modules.

#### 6.2. Manufacturing and Soldering

Push the squeegee to apply the solder paste on the surface of stencil, thus making the paste fill the stencil openings and then penetrate to the PCB. Apply proper force on the squeegee to produce a clean stencil surface on a single pass. To guarantee module soldering quality, the thickness of stencil for the module is recommended to be 0.15–0.18 mm. For more details, see **document [3]**.

The recommended reflow temperature should be 238–246 °C, with 246 °C as the absolute maximum reflow temperature. To avoid damage to the module caused by repeated heating, it is suggested that the module should be mounted only after reflow soldering for the other side of PCB has been completed. The recommended reflow soldering thermal profile (lead-free reflow soldering) and related parameters are shown below.

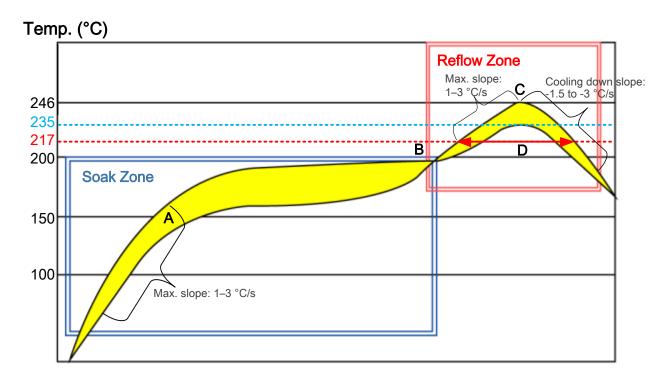


Figure 22: Recommended Reflow Soldering Thermal Profile



**Table 33: Recommended Thermal Profile Parameters** 

Factor	Recommendation
Soak Zone	
Max. slope	1–3 °C/s
Soak time (between A and B: 150 °C and 200 °C)	70–120 s
Reflow Zone	
Max. slope	1–3 °C/s
Reflow time (D: over 217 °C)	40–70 s
Max. temperature	238 °C to 246 °C
Cooling down slope	-1.5 to -3 °C/s
Reflow Cycle	
Max. reflow cycle	1

#### **NOTE**

- 1. During manufacturing and soldering, or any other processes that may contact the module directly, NEVER wipe the module's shielding can with organic solvents, such as acetone, ethyl alcohol, isopropyl alcohol, trichloroethylene, etc. Otherwise, the shielding can may become rusted.
- 2. The shielding can for the module is made of Cupro-Nickel base material. It is tested that after 12 hours' Neutral Salt Spray test, the laser engraved label information on the shielding can is still clearly identifiable and the QR code is still readable, although white rust may be found.
- 3. If a conformal coating is necessary for the module, do NOT use any coating material that may chemically react with the PCB or shielding cover, and prevent the coating material from flowing into the module.
- 4. Avoid using ultrasonic technology for module cleaning since it can damage crystals inside the module.
- 5. Due to the complexity of the SMT process, please contact Quectel Technical Support in advance for any situation that you are not sure about, or any process (e.g. selective soldering, ultrasonic soldering) that is not mentioned in *document [3]*.



#### 6.3. Packaging Specifications

The module adopts carrier tape packaging and details are as follow:

#### 6.3.1. Carrier Tape

Dimension details are as follow:

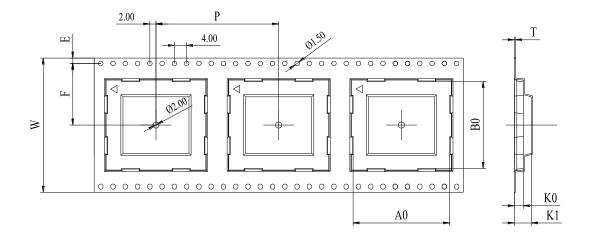


Figure 23: Carrier Tape Dimension Drawing

**Table 34: Carrier Tape Dimension Table (Unit: mm)** 

W	Р	Т	Α0	В0	K0	K1	F	E	
44	32	0.4	18.5	20.5	3	6.8	20.2	1.75	



#### 6.3.2. Plastic Reel

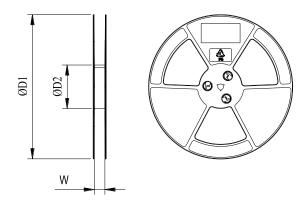


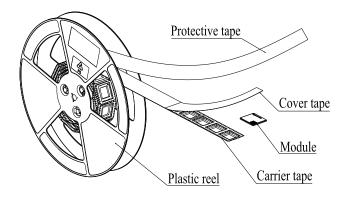
Figure 24: Plastic Reel Dimension Drawing

Table 35: Plastic Reel Dimension Table (Unit: mm)

øD1	øD2	W
330	100	44.5

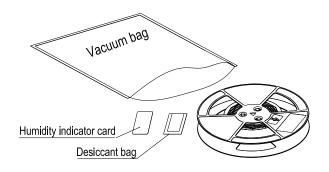


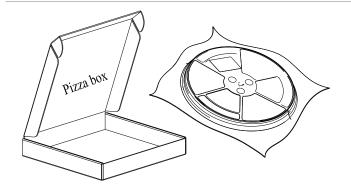
#### 6.3.3. Packaging Process



Place the module into the carrier tape and use the cover tape to cover it; then wind the heat-sealed carrier tape to the plastic reel and use the protective tape for protection. 1 plastic reel can load 250 modules.

Place the packaged plastic reel, 1 humidity indicator card and 1 desiccant bag into a vacuum bag, vacuumize it.





Place the vacuum-packed plastic reel into the pizza box.

Put 4 packaged pizza boxes into 1 carton box and seal it. 1 carton box can pack 1000 modules.

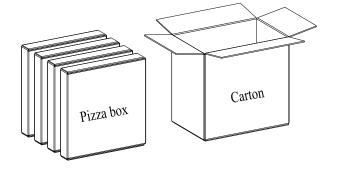


Figure 25: Packaging Process



## 7 Appendix References

#### **Table 36: Reference Documents**

Document Name		
[1] Quectel_FC41D_TE-B_User_Guide		
[2] Quectel_RF_LAYOUT_Application_Note		
[3] Quectel_Module_SMT_Application_Note		
[4] Quectel_FC41D_AT_Commands_Manual		

**Table 37: Terms and Abbreviations** 

previation Des	scription
Acc	cess Point
Blu	etooth Low Energy
SK Bin	ary Phase Shift Keying
K Con	mplementary Code Keying
S Cle	ear To Send
SK Diff	ferential Phase Shift Keying
PSK Diff	ferential Quadrature Reference Phase Shift Keying
) Ele	ctrostatic Discharge
TT Ge	neric Attribute Profile
SK Ga	uss Frequency Shift Keying
D Gro	bund
Hig	h Throughput
PSK Diff  D Ele  IT Ger  SK Gar  D Gro	ferential Quadrature Reference Phase Shift Keying ectrostatic Discharge neric Attribute Profile uss Frequency Shift Keying



IEEE	Institute of Electrical and Electronics Engineers
I/O	Input/Output
Mbps	Megabits per second
MPN	Manufacturer Part Number
QAM	Quadrature Amplitude Modulation
QPSK	Quadrature Phase Shift Keying
RF	Radio Frequency
RH	Relative Humidity
RoHS	Restriction of Hazardous Substances
STA	Station
RTS	Request to Send
RXD	Receive Data (Pin)
SDIO	Secure Digital Input and Output Card
TBD	To Be Determined
TXD	Transmit Data (Pin)
UART	Universal Asynchronous Receiver/Transmitter
USB	Universal Serial Bus
VHT	Very High Throughput
V <sub>IH</sub> max	Maximum High-level Input Voltage
V <sub>IH</sub> min	Minimum High-level Input Voltage
V <sub>IL</sub> max	Maximum Low-level Input Voltage
V <sub>IL</sub> min	Minimum Low-level Input Voltage
V <sub>OL</sub> max	Maximum Low-level Output Voltage
V <sub>OH</sub> min	Minimum High-level Output Voltage
Vnom	Normal Voltage Value
VSWR	Voltage Standing Wave Ratio